

**MOS Transistor**

**Abstract**

A reduced feature size MOS transistor and its method of manufacture is disclosed. The present invention reduces short channel effects but does not include an LDD structure. In an illustrative embodiment, a MOS transistor has a gate length of 1.25  $\mu$ m or less. The exemplary MOS transistor includes a gate oxide that forms a planar and substantially stress free interface with a substrate. As a result of the planarity and substantially stress free nature of the oxide/substrate interface, the incidence of hot carriers, and thereby, deleterious hot carrier effects are reduced. By eliminating the use of the LDD structure, fabrication complexity is reduced and series source-drain resistance is reduced resulting in improved drive current and switching speed.

**BEST AVAILABLE COPY**